UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,643	10/29/2003	Tomohiro Takamatsu	032057	5393

38834 7590 04/06/2007

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
ERDEM, FAZLI	
ART UNIT	**PAPER NUMBER**
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,643	TAKAMATSU ET AL.	
	Examiner	Art Unit	
	Fazli Erdem	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *17-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/07 and 2/9/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's arguments filed on 11/27/2006 have been fully considered and found to be persuasive. However, after further search and consideration and the consideration of the IDS documents filed on 12/09/2006 and 2/7/2007, this action is issued and made non-final.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-9 rejected under 35 U.S.C. 103(a) as being unpatentable over Suenaga et al. (6,239,457) in view of Vente et al. (Journal of Solid State Chemistry, Prior art submitted by the applicant on 12/7/2006)

Regarding Claim 14, in Figs. 1A, 6, 7A, 7B, 8A-8D and 10, Suenaga et al. disclose a semiconductor memory device comprising: an insulating film 102 in Fig 10, formed over a semiconductor substrate 98; an adhesive layer 81 formed on the insulating film and having a surface roughness of 0.79 nm or less (as disclosed in Figs. 7A and 7B); a capacitor lower electrode 11 formed on the adhesive layer, a ferroelectric layer 104 formed on the capacitor lower electrode, and having an ABO3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55 and an upper capacitor electrode 105 formed on the ferroelectric layer. Suenaga et al. fail to disclose the required iridium in the ferroelectric layer. However, Vente et al. discloe a structure chemistry and electronic properties of the hexagonal perovskites BaIrCoO3

which includes Ba in A site, Co in B site and Ir in at least one of A or B site as shown in pages 361-363.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required Ir in A or B sites of ABO3 structure of Suenaga et al. in order to have a increased stability and diffusion characteristics between the lower electrode and the ferroelectric layer of Suenaga et al. since Suenaga et al. discloses that the lower electrode contains Iridium and the integration of Ir in the A site or the B site of ferroelectric layer enhances the diffusion barrier of the ferroelectric layer.

Regarding Claim 2, it is disclosed in Suenaga et al. that ferroelectric layer has preferred the orientation is perpendicular to substrate pane hence 0 degrees inclination from perpendicular direction which would satisfy 3.5 degrees or LESS claim language), a ferroelectric layer 104 formed on the capacitor lower electrode, and having an ABO3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55

Regarding Claim 3, Regarding Claim 13, Fig 3 of Suenaga et al. disclose PZT based ferroelectric layer 104.

Regarding Claim 4, it is disclosed in Suenaga et al. that ferroelectric layer has preferred the orientation is perpendicular to substrate pane hence 0 degrees inclination from perpendicular direction which would satisfy 2.3 degrees or LESS claim language), a ferroelectric layer 104 formed on the capacitor lower electrode, and having an ABO3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55

Regarding Claim 5, in Suenaga et al., lower electrode 11 is Pt or Ir as disclosed column 2 lines 22-33

Regarding Claim 6, Figs. 7A and 7B of Suenaga et al. disclose an adhesive layer having a surface roughness of 0.79 nm or less.

Regarding Claim 8, upper electrode of Suenaga et al. is Pt or Ir as disclosed column 2 lines 22-33

3. Claim 7, rejected under 35 U.S.C. 103(a) as being unpatentable over Suenaga et al. (6,239,457) in view of Vente et al. (Journal of Solid State Chemistry, Prior art submitted by the applicant on 12/7/2006) further in view of Nam et al. (2003/0057464).

Regarding Claim 14, in Figs. 1A, 6, 7A, 7B, 8A-8D and 10, Suenaga et al. disclose a semiconductor memory device comprising: an insulating film 102 in Fig 10, formed over a semiconductor substrate 98; an adhesive layer 81 formed on the insulating film and having a surface roughness of 0.79 nm or less (as disclosed in Figs. 7A and 7B); a capacitor lower electrode 11 formed on the adhesive layer, a ferroelectric layer 104 formed on the capacitor lower electrode, and having an ABO3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55 and an upper capacitor electrode 105 formed on the ferroelectric layer.. Vente et al. discloe a structure chemistry and electronic properties of the hexagonal perovskites BaIrCoO3 which includes Ba in A site, Co in B site and Ir in at least one of A or B site as shown in pages 361-363. Suenaga et al. and Vente et al. combination fail to disclose the requried Al2O3/alumina adhesive layer. However, Nam disclosed a ferroelectric memory device and

method of fabricating the same where in paragraph 035, the required Al2O3 adhesive layer is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required alumina adhesive layer in Suenaga et al. and Verde et al. combination as taught by Nam, in order to have a ferroelectric memory device with better adhesion properties.

4. Claims 9-13 rejected under 35 U.S.C. 103(a) as being unpatentable over Suenaga et al. (6,239,457).

Regarding Claim 9, in Figs. 1A, 6, 7A, 7B, 8A-8D and 10, Suenaga et al. disclose a semiconductor memory device comprising: an insulating film 102 in Fig 10, formed over a semiconductor substrate 98; an adhesive layer 81 formed on the insulating film and having a surface roughness of 0.79 nm or less (as disclosed in Figs. 7A and 7B); a capacitor lower electrode 11 formed on the adhesive layer, and having an (111) orientation that is in perpendicular direction (as disclosed in column 2, lines 22-33. It is also disclosed the preferably the orientation is perpendicular to substrate pane hence 0 degrees inclination from perpendicular direction which would satisfy 2.3 degrees or LESS claim language), a ferroelectric layer 104 formed on the capacitor lower electrode, and having an ABO3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55 and an upper capacitor electrode 105 formed on the ferroelectric layer.

Regarding Claim 10, lower electrode direction is specified as perpendicular to the substrate plane which means it has 0 degrees inclination from the perpendicular which would satisfy 3.5 degrees or LESS claim language. (column 2, lines 22-33)

Regarding Claim 11, ferroelectric layer 104 has (111) orientation that is preferable perpendicular to the substrate plane, i.e. 0 degrees inclination from the perpendicular direction, which satisfies the claim language of 3.5 degrees or LESS requirement, a ferroelectric layer 104 formed on the capacitor lower electrode, and having an ABO3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55 and an upper capacitor electrode 105 formed on the ferroelectric layer.

Regarding Claim 12, lower electrode 11 is Pt or Ir as disclosed column 2 lines 22-33

Regarding Claim 13, Fig 3 discloses PZT based ferroelectric layer 104.

5. Claims 14-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Suenaga et al. (6,239,457) in view of Kim et al. (6,737,694).

Regarding Claim 14, in Figs. 1A, 6, 7A, 7B, 8A-8D and 10, Suenaga et al. disclose a semiconductor memory device comprising: an insulating film 102 in Fig 10, formed over a semiconductor substrate 98; an adhesive layer 81 formed on the insulating film and having a surface roughness of 0.79 nm or less (as disclosed in Figs. 7A and 7B); a capacitor lower

electrode 11 formed on the adhesive layer, and having an (111) orientation that is in perpendicular direction (as disclosed in column 2, lines 22-33. It is also disclosed the preferably the orientation is perpendicular to substrate pane hence 0 degrees inclination from perpendicular direction which would satisfy 2.3 degrees or LESS claim language), a ferroelectric layer 104 formed on the capacitor lower electrode, and having an ABO3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr) as disclosed in column 2, lines 34-55 and an upper capacitor electrode 105 formed on the ferroelectric layer. Suenaga et al. fail to disclose the required contact hole and the conductive plug structure. However, Kim et al. disclose a ferroelectric memory device and method of forming the same where in Fig. 2 it is disclose a hole 210b formed in the insulating film 208 under and the adhesive layer 212b (which includes a stacked layer for adhesive purposes as shown in column 7, lines 35-50), under the lower electrode 220, a conductive plug is formed in the hole (shaded area 210b is conductive plug) and connected to the lower electrode 220.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required conductive plug in Suenaga et al. as taught by Kim et al. in order to have the ferroelectric capacitor structgure of Suenaga et al. to function properly in a ferroelectric memory device.

Regarding Claim 15, in Fig. 2 of Kim et al., layer 214 acts as the barrier layer and is located between the lower electrode 220 and the conductive plug 212b.

Regarding Claim 16, layer 214 is part of the lower electrode 220 as shown in Fig 2 of Kim et al. since it is in contact with lower electrode.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FE
March 27, 2007

SUE A. PURVIS
SUPERVISORY PATENT EXAMINER